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GROUP 2700

IN THE UNITED STATES

PATENT AND TRADEMARK OFFICE

Applicant(S):	Goran Devic
Serial NO.:	08/818,053
Filing DATE:	March 14, 1997
Title:	METHOD AND Apparatus FOR SHORTENING DISPLAY LIST INSTRUCTIONS
Examiner:	K. Tung
Group Art Unit:	~~2773~~ 2776
Atty. Dkt. No.:	3378

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Assistant Commissioner For Patents, Washington, D.C. 20231, on the date shown below:

Dated: _____ By: _____ , Reg. No.:

ASSISTANT COMMISSIONER FOR PATENTS
WASHINGTON, D.C. 20231

ASSOCIATE POWER OF ATTORNEY

SIR:

The following person is hereby appointed as Associate Attorney to prosecute the above-referenced application and any continuing applications, to maintain the ensuing patent, and to transact all other business in the U.S. Patent and Trademark Office connected therewith:

Name	Registration Number
Leif R. Sloan	37,942

Respectfully submitted,
X

Dated: Aug 25, 1999

By: _____

Greg T. Sueoka, Reg. No.: 35,800
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Attn: Examiner Kee M. Tung
(703) 305-9660
Re: Proposed claim for 08/818,053

A graphics system for processing parameter values of graphics primitives in a display list, wherein the display list is shortened to enable fast processing time while maintaining the quality of information contained in the display list, the graphics system comprising:

a register file, for storing at least one set of parameter values, the register file comprising a plurality of registers;

a partition table comprising a set of addressable storage locations, the contents of each storage location specifying a starting register file address;

a load instruction unit, for storing an instruction having an opcode portion that specifies a rendering operation, a partition portion that specifies a partition table address, and a write-enable portion that spans a plurality of bits, wherein a first bit in association with the partition portion corresponds to a target starting register file address and subsequent bits sequentially correspond to register file addresses that follow the target starting register file address;

a shifter coupled to receive the write-enable portion, for sequentially performing single-bit shifts upon the contents of the write-enable portion; and

a rendering parameter storage controller coupled to the shifter and the register file, for sequentially stepping through register file addresses corresponding to bits spanning the write-enable portion, and storing a parameter value in the register file in response to a bit under consideration by the shifter having a predetermined value.

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